IN THE CLAIMS:

Please amend claims 1, 16, and 18 as follows:

1. (Currently amended) A method of recovering timing information over multiple asynchronous packet networks, each having its own time grid, comprising:

transmitting timestamped packets between a sender on a first said network and a receiver on a second said network;

transporting timing information between the sender and receiver as a modulated signal comprising a modulation in the ~~time of departure or~~ rate of sending out the timestamped packets transmitted between the sender and receiver;

extracting said timing information from the packets arriving at the receiver; and

using said timing information at the receiver to align the time grid at the receiver with the time grid at the sender, and

wherein said modulated signal is manifested as an offset in the rate of transmission of packets from the sender, said offset being an odd fraction *f* of a cycle of a clock signal such that the timing error at the receiver contains only high frequency components, and wherein the packet rate is offset by an amount equal to the ratio of the packet cycle and clock cycle multiplied by *f*.

2. (Original) The method of claim 1, wherein said modulated signal is frequency or phase modulated.

3. Canceled.

4. Canceled.

5. (Previously presented) The method of claim 7, wherein *f* is 5/32.

6. (Previously presented) The method of claim 7, wherein *f* is 27/32.

7. (Previously presented) A method of recovering timing information in a packet network, wherein a modulated signal is used to transport additional information required for clock recovery between the sender and receiver across the network, wherein said modulated signal is manifested as an offset in the rate of transmission of packets from the sender, said offset being an odd fraction *f* of a cycle of a clock signal such that the timing error at the receiver contains only high frequency components, and wherein the packet rate is offset by an amount equal to the ratio of the packet cycle and clock cycle multiplied by *f*.

8. (Previously presented) The method of claim 7, wherein said high frequency components are filtered out at the receiver.

9. (Original) The method of claim 1, wherein a phase locked loop is provided at the receiver to remove timing errors arising between the last node in the path of a packet across the network and the receiver.

10. (Original) The method of claim 1, wherein said modulated signal uses sinusoidal modulation.

11. (Original) The method of claim 1, wherein said modulated signal is the summation of two sinusoidal waveforms.

12. (Original) The method of claim 1, wherein said modulated signal uses a sawtooth or form of modulation.

13. (Original) The method of claim 1, wherein said modulated signal uses pseudo-random modulation.

14. (Previously presented) In a packet network linking a sender and receiver, an apparatus for recovering timing information across the network at the receiver comprising:

a modulator at the sender for sending a modulated signal across the network

conveying timing information; and

a clock recovery unit at the receiver using said modulated signal to improve the accuracy of the recovered clock; and

a control unit coupled to said modulator for varying the precise time of departure of outgoing packets to provide said modulated signal, said control unit varying the time of transmission of said packets to provide an offset in rate the transmission of said packets,

wherein said offset is an odd fraction *f* of a cycle of a clock signal such that the timing error at the receiver contains only high frequency components; and

wherein the packet rate is offset by an amount equal to the ratio of the packet cycle and clock cycle multiplied by *f*.

15. Canceled

16. (Currently amended) The apparatus as claimed in claim ~~15~~ 14, wherein said recovery unit includes a synchronous detector for determining the precise time of arrival of an incoming packet.

17. (Original) The apparatus as claimed in claim 16, wherein the sender and receiver each include a local timebase as a reference.

18. (Currently amended) The apparatus as claimed in claim ~~15~~ 14, wherein said modulator is connected to a network interface unit.

19. Canceled.

20. Canceled

21. Canceled.

22. (Previously presented) The apparatus of claim 14, wherein *f* is 5/32.

23. (Previously presented) The apparatus of claim 14, wherein *f* is 27/32.

24. (Original) The apparatus of claim 14 further comprising a phase locked loop at the receiver for removing errors arising in the last link of the network before the receiver.